cont, C3

77. A device according to claim 32 wherein at least one of said semiconductor islands comprises boron at a concentration in the range of 1×10^{15} to 1×10^{18} cm^{-3}.

78. A device according to claim 41 wherein each of the channel semiconductor layers comprises boron at a concentration in the range of 1×10^{15} to 1×10^{18} cm^{-3}.--

REMARKS

Applicant would like to thank the Examiner for the consideration given the present application. The Office Action of **October 18, 2001**, has been received and its contents carefully noted. Applicant respectfully submits that this response is timely filed and fully responsive to the Office Action. Claims 21-41 and 43-66 were pending in the present application prior to the aforementioned amendment. By the above actions, claims 21-32 and 41 are amended and new claims 67-78 are added to recite protection to which Applicant is already entitled. Accordingly, Claims 21-41 and 43-66 are currently pending in the present application, and are believed to be in condition for allowance at least for the reasons advanced hereinbelow.

A. Double Patenting Rejection

Initially, the Office Action rejects claims 21-41 and 43-66 under 35 U.S.C. §101 as claiming the same subject matter as that of claims 1-46 of prior U.S. Patent No. 6,023,075. Applicant respectfully request that this rejection be held in abeyance until an indication of allowability has been received.

B. 35 U.S.C. §103(a) Rejections

The Office Action further rejects claims 21-33, 41, 43, 44, 49, 52, 53, 56, 61-66 under 35 U.S.C. §103(a) as unpatentable over ***Chang '781*** in view of ***Misawa '826*** and

Yamazaki JP '173, claims 21-41, 43-56 and 61-66 stand rejected under 35 U.S.C. §103(a) as unpatentable over ***Chang '781*** in view of ***Misawa '826*** and ***Yamazaki JP '173***, and further in view of ***Baldi '552***, and claims 21-41 and 43-66 under 35 U.S.C. §103(a) as unpatentable over ***Misawa '826*** in view of ***Chang '781***, ***Yamazaki JP '173*** and ***Baldi '552***, and further in view of ***Sumiyoshi '134*** and ***Akiyama***. Applicant traverses these rejections at least for the reasons solicited hereinbelow.

The claimed invention is directed generally to an active matrix display device having a pixel portion and a driver circuit portion, the driver circuit portion including at least one pair of complementary p-channel and n-channel thin film transistors, and the pixel portion including at least one thin film transistor. More particularly, the claimed invention is directed to such an active matrix display device whereby each transistor includes, *inter alia*, a crystalline semiconductor island on an insulating surface, the semiconductor island having source and drain regions and a channel region, a gate insulating film adjacent to at least the channel region, a gate electrode adjacent to the gate insulating film, and <u>a leveling film covering each of the thin film transistors in both of the pixel portion and a part of the driver circuit portion</u>.

As the Examiner well knows, in formulating a rejection under 35 USC §103, the following four-level factual inquiry must be conducted: (1) determine the scope and content of the prior art; (2) ascertain differences between the claimed invention and the prior art; (3) resolve the level of ordinary skill in the pertinent art; and (4) evaluate objective evidence of non-obviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). In essence, to establish a *prima facie* case of obviousness, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 180 USPQ 580 (CCPA 1974).

Applicant respectfully contends that the prior art of record fails to expressly teach or implicitly suggest each an every claim limitation necessary to support a finding of *prima facie* obviousness under §103.

Referring now to the Office Action, in which ***Misawa '826*** is combined with the teachings of ***Chang '781*** since it allegedly discloses an "insulating film 84, 95 which covers both the pixel and the driver transistors and can function or be labeled as a leveling film." Applicant respectfully traverses this finding in stating that ***Misawa '826*** fails to expressly teach or implicitly suggest <u>a leveling film covering each of the thin film transistors in both of the pixel portion and a part of the driver circuit portion</u>, as presently set forth in the claimed invention. In order to render an invention obvious, the prior art must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). In Applicant's review of ***Misawa '826***, there is no clear teaching or inherent disclosure of such a feature. Applicant respectfully request that the Examiner either provide evidence showing that ***Misawa '826*** suggests that the insulating film 84, 95 may additionally function or be labeled as a leveling film or withdraw the rejection.

The Office Action combines ***Misawa '826*** with the teachings of ***Sumiyoshi '134*** and ***Akiyama***, which allegedly suggest "resin leveling or passivation films over transistors." Inasmuch as the base ***Misawa '826*** reference fails to expressly teach or implicitly suggest <u>a leveling film covering each of the thin film transistors in both of the pixel portion and a part of the driver circuit portion</u>, Applicant respectfully contends that the proposed combination is improper as failing to render each and every claimed feature obvious.

Notwithstanding this contention, Applicant further contends that there is a lack of suggestion in either of ***Misawa '826***, ***Sumiyoshi '134*** and ***Akiyama*** to combine their respective teachings in such a manner that would render the claimed invention obvious. In order to render an invention *prima facie*, there must be some teaching, suggestion, or motivation to combine or modify the teachings of the prior art to produce the claimed invention, found either in the references themselves or in the knowledge generally available to a skilled artisan. *In re Fine*, 837 F.2d 1071, 5 USPQ.2d 1596 (Fed. Cir.

1988). The Office Action finds that the teachings of ***Sumiyoshi '134*** and ***Akiyama*** may be combined with ***Misawa '826*** in spite of a lack of suggestion in either of the references for making the combination. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection.

Accordingly, since the prior art rejections fail to expressly teach or inherently describe each and every claim limitation necessary to support a finding of *prima facie* obviousness under §103, Applicant respectfully requests that the rejections be reconsidered and withdrawn. If the Examiner believes further discussions with Applicants' representative would be beneficial in this case, he is invited to contact the undersigned.

Respectfully submitted,

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Marked-up copy of amended claims

21. (Amended) An active matrix display device having a pixel portion and a driver circuit portion, said driver circuit portion including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and a part of the driver circuit portion~~,~~

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V{\cdot}sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V{\cdot}sec$ or more,

[wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3},] and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less.

22. (Amended) A semiconductor circuit having a pixel portion and a shift register, said shift register including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor. each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and the shift register,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more,

[wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18} cm^{-3}$,] and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less.

23. (Amended) A semiconductor circuit having a pixel portion and an inverter, said inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and the inverter,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more,

[wherein at least one of said semiconductor islands comprises boron at a concentration in the range of 1×10^{15} to $1x10^{18}$ cm^{-3},] and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less.

24. (Amended) A semiconductor circuit having a pixel portion and a clocked inverter, said clocked inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and the clocked inverter,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more,

[wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3},] and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less.

25. (Amended) An active matrix display device having a pixel portion and a driver circuit portion, said driver circuit portion including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region; and a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and a part of the driver circuit portion,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more,

[wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3} to control an absolute value of a threshold voltage of said n-channel thin film transistor to be substantially the same as an absolute value of a threshold voltage of said p-channel thin film transistor,] and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less.

26. (Amended) A semiconductor circuit having a pixel portion and a shift register, said shift register including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and in the shift register,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V{\cdot}sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V{\cdot}sec$ or more,

[wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3} to control an absolute value of a threshold voltage of said n-channel thin film transistor to be substantially the same as an absolute value of a threshold voltage of said p-channel thin film transistor,] and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less.

27. (Amended) A semiconductor circuit having a pixel portion and an inverter, said inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and the inverter,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 cm2/V·sec or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 cm2/V·sec or more,

[wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3} to control an absolute value of a

threshold voltage of said n-channel thin film transistor to be substantially same the as an absolute value of a threshold voltage of said p-channel thin film transistor,] and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less.

28. (Amended) A semiconductor circuit having a pixel portion and a clocked inverter, said clocked inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and the clocked inverter,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V{\cdot}sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V{\cdot}sec$ or more,

[wherein at least one of said semiconductor islands comprises boron at a concentration in the range of 1×10^{15} to $1 x 10^{18}$ cm^{-3} to control an absolute value of a threshold voltage of said n-channel thin film transistor to be substantially the same as an absolute value of a threshold voltage of said p-channel thin film transistor,] and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less.

29. (Amended) An active matrix display device having a pixel portion and a driver circuit portion, said driver circuit portion including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said p-channel and n-channel thin film transistors in both of the pixel portion and a part of the driver circuit portion,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V{\cdot}sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V{\cdot}sec$ or more,

[wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3},]

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein each of said semiconductor islands comprises oxygen at a concentration not higher than $7x10^{19}$ cm^{-3}.

30. (Amended) A semiconductor circuit having a pixel portion and a shift register, said shift register including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and the shift register,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more,

[wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3},]

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein each of said semiconductor islands comprises oxygen at a concentration not higher than $7x10^{19}$ cm^{-3}.

31. (Amended) A semiconductor circuit having a pixel portion and an inverter, said inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and the inverter,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more,

[wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3},]

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein each of said semiconductor islands comprises oxygen at a concentration not higher than $7x10^{19}$ cm^{-3}.

32. (Amended) A semiconductor circuit having a pixel portion and a clocked inverter, said clocked inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and the clocked inverter,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more,

[wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3},]

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein each of said semiconductor islands comprises oxygen at a concentration not higher than 7×10^{19} cm^{-3}.

41. (Amended) An active matrix display device including a pixel portion and a driver circuit portion comprising:

a plurality of pixel electrodes formed on an insulating surface;

a first plurality of thin film transistors being formed in the pixel portion on said insulating surface and being connected to said pixel electrodes;

a second plurality of thin film transistors being formed in the driver circuit portion on said insulating surface, said second plurality of thin film transistors including at least one pair of complementary p-channel and n-channel thin film transistors; and

a leveling film covering both of the first and second plurality of thin film transistors in the pixel portion and a part of the driver circuit portion,

wherein said second plurality of thin film transistors in said driver circuit include channel semiconductor layers having at least one of an electron mobility 15 $cm^2/V \cdot sec$ or more and a hole mobility of 10 $cm^2/V \cdot sec$ or more,

[wherein each of the channel semiconductor layers comprises boron at a concentration in the range of 1×10^{15} to 1×10^{18} cm^{-3},] and

wherein each of said channel semiconductor layers has a thickness of 5000 Å or less.